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DESIGN AND IMPLEMENTATION OF AC-DC-DC CONVERTER PROVIDING MULTICHANNEL FIXED AND VARIABLE DC OUTPUT VOLTAGES

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INTRODUCTION:

Today in electrical power conversion system, the power electronics plays a major role, also gives various answer to solve problems associated with conventional power supplies. The ac/dc converters have received much attention due to cost effectiveness, compact size.The boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation. Their intermediate bus voltage is usually greater than the line input voltage. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage, this high intermediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell, extremely narrow duty cycle is needed for the conversion.

This leads to poor circuit efficiency and limits the input voltage range for getting better performance. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, no isolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually adde resulting in more component counts. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection.

To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported. Although the recently reported IBoBuBo converter is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters employ different PFC cells to reduce the intermediate bus voltage. Among those converters, [1] and [2] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable.

II.PROPOSED METHOD

In the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [3] and [4] process power at least twice resulting in low power efficiency. Moreover, the reported converters, in [5], and [6], consist of two active switches leading to more complicated gate control.

Apart from reducing the intermediate bus voltage, the converter in [7] employs resonant technique to further

increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in this paper, an integrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage. To sum up, the converter is able to achieve:

- ✓ Low intermediate Output voltages in the absence of transformer.
- ✓ Simple control structure with a single-switch.
- ✓ Positive output voltage.
- ✓ High conversion efficiency due to part of input power is processed once
- ✓ Input surge current protection because of series connection of input source and switch.

III.AC/DC CONVERTER SYSTEM

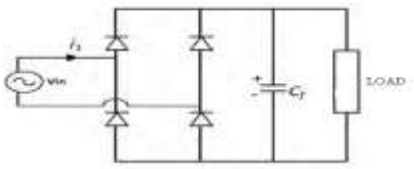


Figure 2.1. Diode bridge rectifier

The diode bridge rectifier, shown in Fig.2.1 has non-sinusoidal line current. This is because most loads require a supply voltage with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor Cf. Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with an important harmonic content.

Two common reasons for including the dc-side filter:

1. Obtain good dc output voltage and acceptable ac line current waveform.

2. Filter conducted EMI (Electromagnetic Interference) generated by dc load.

Power factor is defined as the ratio of active power (P) to the apparent power(S).When an electric load has a PF lower than 1, the apparent power delivered to the load is greater than the real power that the load consumes. Only the real power is capable of doing work, but the apparent power determines the amount of current that flows into the load, for a given load voltage. The basic idea of PFC is design circuits with certain means to force the line current to follow the waveform of the line voltage. Because of the nature of PFC, there exists an unbalance of instantaneous power between the input power, which is an alternative quantity with two times the line frequency, and its dc output power. Therefore, power factor correction involves processing the input power in certain way that it stores the excessive input energy when the input power is larger than the dc output power, and releases the stored energy when the input power is less than the dc output power. To accomplish the above task, at least one energy storage element must be included in the PFC circuit.

Some assumptions were made to analyze the circuit

which are the following:-

- ✓ Load is purely resistive.
- ✓ Ideal filter components.
- ✓ The forward voltage drop and reverse leakage current of diodes are neglected.

Four different passive power factor improvement topologies for low power output with 220volt/50 Hz ac

input are

- ✓ Conventional single phase diode rectifier with filter capacitor.
- ✓ Single phase diode rectifier with LC filter.
- ✓ Single phase diode rectifier circuit with parallel input resonant filter.

Single phase diode rectifier circuit with series input resonant filter.

IV.INTERGRATED BUCK–BUCK–BOOST CONVERTER

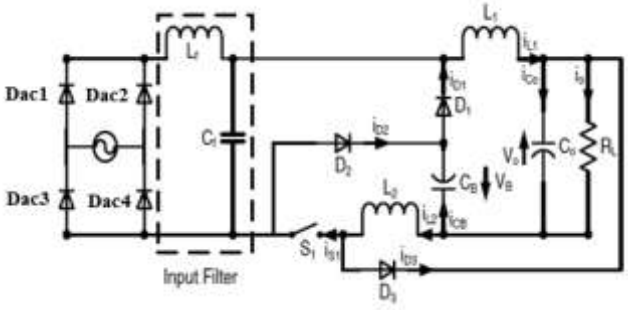


Figure 3.1 Intergrated Buck–Buck–Boost Converter

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (*L*1 , *S*1 , *D*1 , *Co* , and *CB*) and a buck–boost dc/dc cell (*L*2 , *S*1 , *D*2 , *D*3 , *Co* , and *CB*) is illustrated in Fig. 3.1. Although L_2 is on the returnpath of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not considered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle *t*0. Due to the characteristic of buck PFC cell, there are two operating modes in the circuit. Fig 3.2 shows the output waveform of voltage and current.

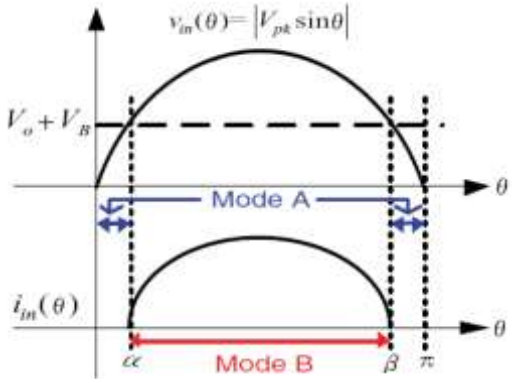


Figure 3.2 output waveform of voltage and current

3.2 VARIOUS MODES OF OPERATION

3.2.1 ModeA **(vin (*θ*)≤*V*$_B$ + *Vo*):**When the input voltage *v*in (*θ*) is smaller than the sum of intermediate bus voltage V_B, and output voltage *Vo*, the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage [8], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 3.2 (mode B). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 3.3, 3.4, and 3.5 Fig. 3.6 shows its key current waveforms.

Stage 1 (period d_1 Ts)

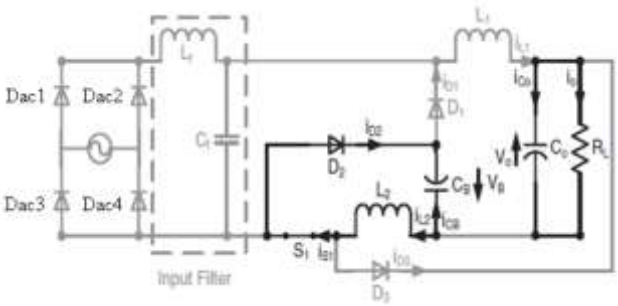


Figure 3.3 MODE A STAGE 1

In fig 3.3 during this period d_1Ts No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4),Filter circuit and inductor L_1. When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor *Co* delivers power to the load.

Stage 2 (period **d_2Ts)**

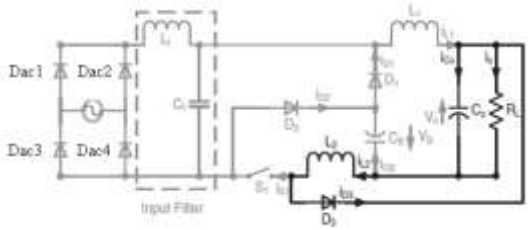


Figure 3.4 MODE A STAGE 2

In fig 3.4 during this period d_2Ts No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4) Filter circuit and inductor L_1, D_1, D_2 and C_B. When switch S_1 is switched OFF, Diode D_3 becomes forward biased and energy stored in L_2 is released to *Co* and the load.

Stage 3 (period d_3T_s - d_4T_s)

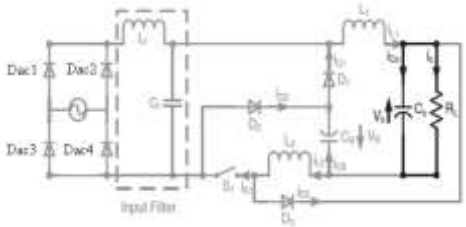


Figure 3.5 MODE A STAGE 3

In fig 3.5 during this period d_2T_s No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4) Filter circuit and inductor L_1, L_2, D_1, D_2 and C_B. The inductor current i_{L2} is totally discharged and only *Co* sustains the load current.

Mode A Key Waveform

- ✓ During period 1 current charges to its peak value as shown in the wave form.

- ✓ During period 2 current discharges to zero value as shown in the wave form.
- ✓ During period 3 and 4 it is negative as shown in the wave form.

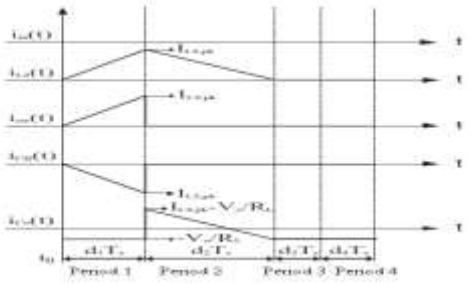


Figure 3.6 MODE A KEY WAVEFORM

*3.2.2 Mode B (vin (θ) > VB + Vo):*This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 3.7, 3.8, 3.9, and 3.10. The key waveforms are shown in Fig. 3.11.

*Stage 1 (period d1Ts)***)**In fig 3.7 when switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage (*v*in (*θ*) − V_B − *Vo*), while diode D_2 is conducting. No conduction in D_1 and D_3.

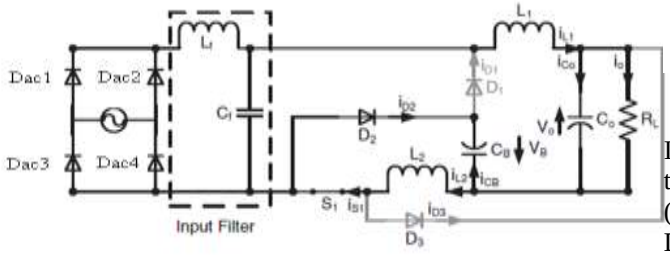


Figure 3.7 MODE B STAGE 1

Stage 2 (period *d2Ts*)

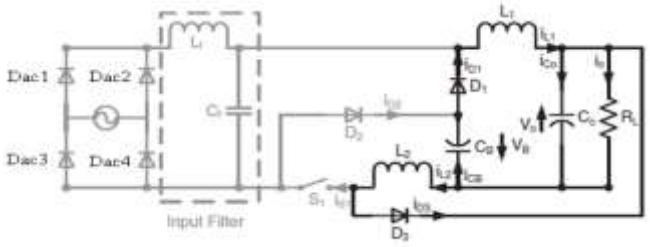


Figure 3.8 MODE B STAGE 2

In fig 3.8 when switch S_1 is switched OFF, inductor current iL_1 decreases linearly to charge C_B and *C*o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to *Co* and the current is supplied to the load through diode D_3. This stage ends once inductor L_2 is fully discharged. During this period d_2Ts No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4) Filter circuit and Diode D_2.

Stage 3 (period d_3T_s)

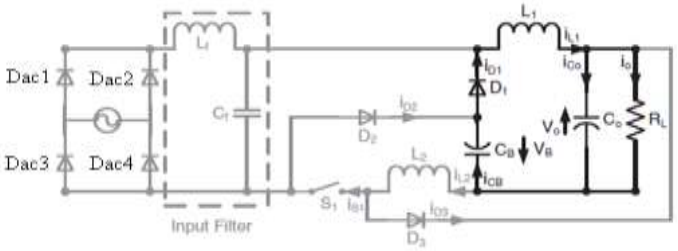


Figure 3.9 MODE B STAGE 3

In fig 3.9 during this period d_3T_s No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4), Filter circuit and inductor L_2, D_2 and D_3.Inductor L_1 continues to deliver current to *Co* and the load until its current reaches zero.

Stage 4 (period *d4Ts*)

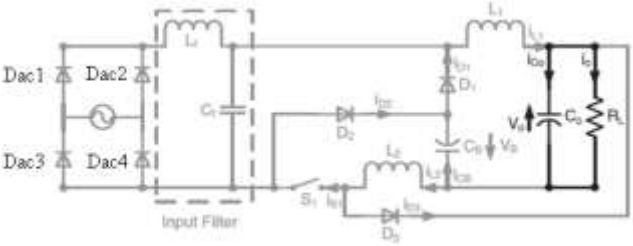


Figure 3.10 MODE B STAGE 4

In fig3.10 Only *Co* delivers all the output power. During this period d_4T_s No current will be flowing in the rectifier (Dac1, Dac2, Dac3, Dac4), Filter circuit, inductor L_1, L_2, D_1 and D_3.

Mode B Key Waveform

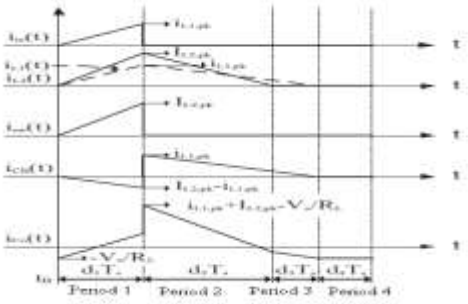
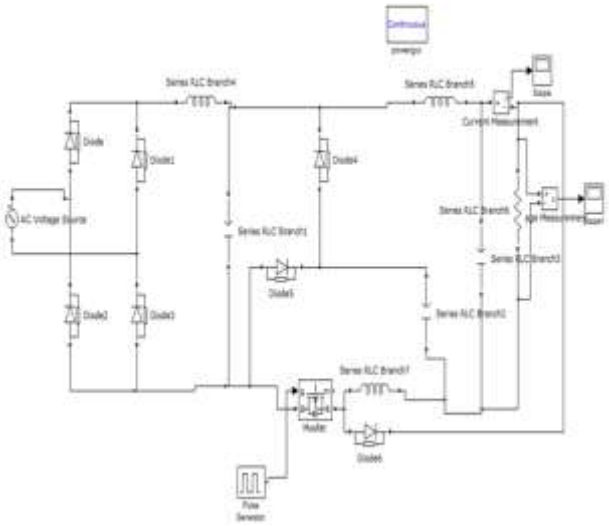


Figure 3.11 MODE B KEY WAVEFORM

SIMULATION OF BUCK BOOST CONVERTER



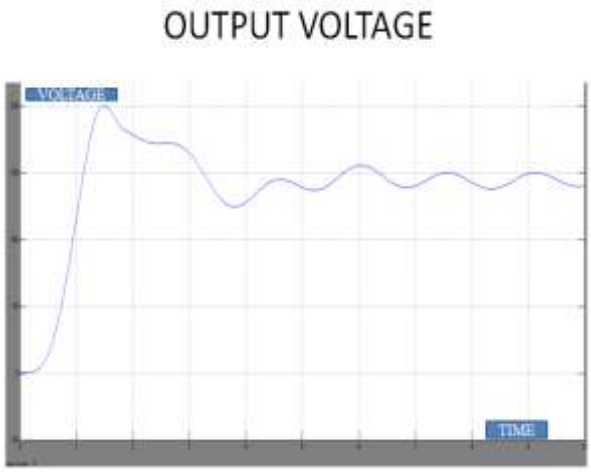
Specifications (Mode A)

Inductor = 1H
Capacitor = 0.1F
Input Voltage=230V ac
Output Voltage = 120.15 V
Input Current =1.46 A
Output Current = 20.04A

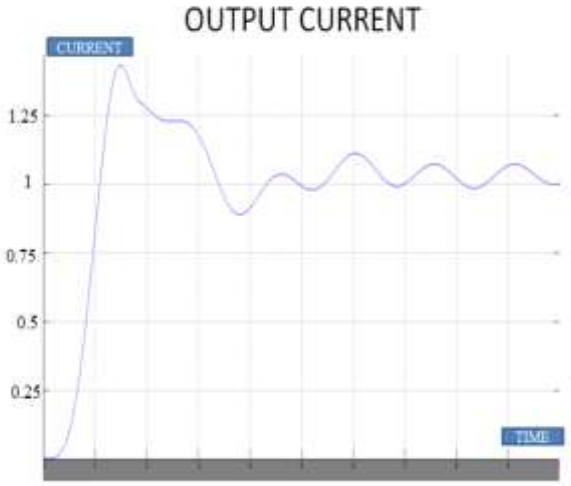
Specifications (Mode B)

Inductor = 1H
Capacitor = 0.1F
Input Voltage=230V ac
Output Voltage = 160.5 V
Input Current =1.20 A
Output Current = 15.8A

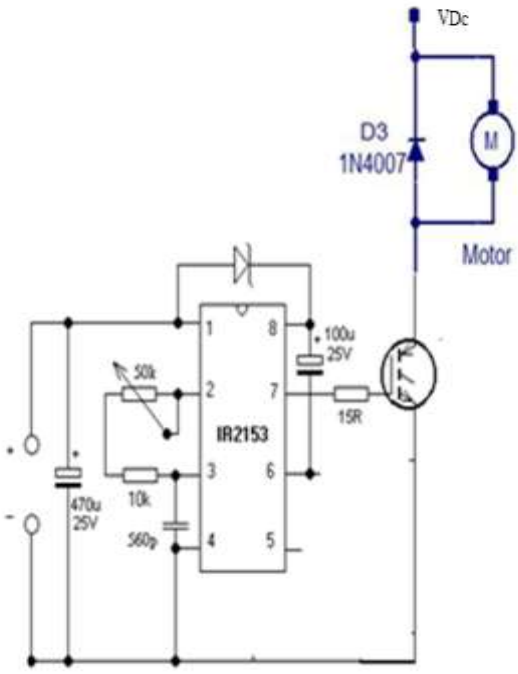
OUTPUT VOLTAGE



V. OUTPUT CURRENT



VI. HARDWARE DESIGN



HARDWARE

VII.RESULTS AND DISCUSSION

In mode A the voltage is greater than mode B voltage. But the current is increased in mode A.The inductor and capacitor values are remain constant.

TABLE 3. SIMULATION RESULT COMPARISON

For M=0.1

	V_{IN}	V_O	I_O
BOOST CONVERTER	180	190	1.15
	200	215	1.3
	250	285	1.2
BUCK CONVERTER	180	115	1.1
	200	180	0.8
	250	240	0.6

For M=0.2

	V_{IN}	V_O	I_O
BOOST CONVERTER	180	195	1.95
	200	225	1.48
	250	260	1.38
BUCK CONVERTER	180	127	1.28
	200	**195**	**0.98**
	250	**245**	**1.4**

CONCLUSION

The proposed Integrated Buck Buck Boost Converter single-stage ac/dc converter has been experimentally verified, and the results have shown good agreements with the predicted values. The intermediate bus voltage of the circuit is able to keep below150V at all input and output conditions, and is lower than that of the most reported converters.

Thus, the lower voltage rating of capacitor can be used. Moreover,the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of transformer, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protection. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency.

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